IN THE CLAIMS

1. (Currently Amended) A wide bandwidth phase-lock loop circuit, comprising:

a frequency detector arranged to measure an input signal of unknown frequency to detect frequency information of ~~an~~ the input signal, the input signal being variable in frequency over a plurality of frequency ranges;

a frequency range selector connected to the frequency detector; and

a phase-locked loop connected to the frequency range selector and capable of ~~operating~~ phase-locking with the input signal when configured to do so for each of ~~in a~~ the plurality of frequency ranges, wherein the frequency range selector automatically determines the frequency range for the input signal and configures the phase-locked loop to generate an output signal within one of the plurality of frequency ranges based on the frequency information of the input signal.

2. (Original) The circuit of claim 1, further comprising a divider connected to the phase-locked loop and configurable to divide a frequency of the output signal generated by the phase-locked loop.

3. (Currently Amended) The circuit of claim 1, wherein the frequency range selector employs frequency range hysteresis whereby the plurality of frequency ranges are overlapping and the frequency range selector does not reconfigure the phase-locked loop to change frequency ranges when frequencies of the input signal are in overlapping frequency ranges.

4. (Original) The circuit of claim 1, wherein the frequency detector comprises a zero-crossing synchronizer that synchronizes the input signal to a clock signal.

5. (Original) The circuit of claim 1, wherein the frequency detector comprises a zero-crossing counter that counts zero-crossings of the input signal.

6. (Original) The circuit of claim 1, wherein the frequency range selector comprises a range detector for detecting which one of the plurality of frequency ranges is an appropriate frequency range based on the frequency information of the input signal.

7. (Currently Amended) The circuit of claim 6, wherein the frequency range selector further comprises a range selector programmed for confirming that at least two consecutive detections are in the same frequency range prior to changing the frequency range ~~detected by the range delector~~.

8. (Original) The circuit of claim 1, further comprising a voltage comparator connected to the frequency detector and adapted to condition a wave form of the input signal.

9. (Currently Amended) A method of phase locking ~~a~~ an input signal having a wide range of frequencies, comprising:

measuring ~~obtaining~~ frequency information of ~~an~~ the input signal;

selecting one out of a plurality of frequency ranges based on the frequency information obtained by said step of measuring ~~of the input signal~~; and

generating an output signal by phase-locking to the input signal within the selected frequency range.

10. (Original) The method of claim 9, further comprising dividing a frequency of the output signal.

11. (Original) The method of claim 9, further comprising employing frequency range hysteresis.

12. (Currently Amended) The method of claim 9, further comprising confirming the selected frequency range by comparing results of at least two of said steps of measuring prior to changing the selected frequency range.

13. (Original) The method of claim 9, further comprising synchronizing the input signal to a clock signal.

14. (Original) The method of claim 9, further comprising counting zero-crossings of the input signal.

15. (Original) The method of claim 9, further comprising conditioning a wave form of the input signal.

16. (Currently Amended) A phase-lock loop circuit having a wide bandwidth, comprising:

means for measuring ~~obtaining~~ frequency information of an input signal;

means for selecting one out of a plurality of frequency ranges based on the measured frequency information of the input signal; and

means for ~~generating~~ phase-locking to said input signal to thereby generate an output signal in the selected frequency range.

17. (Original) The circuit of claim 16, further comprising means for dividing a frequency of the output signal.

18. (Original) The circuit of claim 16, wherein the means for selecting employs frequency range hysteresis.

19. (Original) The circuit of claim 16, wherein the means for selecting confirms the selected frequency range.

20. (Currently Amended) The circuit of claim 16, wherein the means for measuring ~~obtaining~~ synchronizes the input signal to a clock signal.

21. (Currently Amended) The circuit of claim 16, wherein the means for ~~obtaining~~ measuring counts zero-crossings of the input signal.

22. (Currently Amended) The circuit of claim 16, further comprising means for conditioning a wave form of the input signal.

23. (Original) A wide bandwidth phase-lock loop circuit, comprising:

a frequency detector arranged to detect frequency information for an input signal, the frequency detector having a zero-crossing synchronizer for synchronizing the input signal to a clock signal and a zero-crossing counter for counting zero-crossings of the input signal;

a frequency range selector connected to the frequency detector and having a range detector and a range selector, wherein the range detector detects which one of a plurality of frequency ranges is an appropriate frequency range based on the frequency information of the input signal, and wherein the range selector confirms the frequency range detected by the range detector;

a phase-locked loop connected to the frequency range selector and configured by the frequency range selector to generate an output signal in the frequency range detected by the range detector, wherein the frequency range selector employs frequency range hysteresis;

a divider for dividing a frequency of the output signal; and

a voltage comparator for conditioning a wave form of the input signal.